RDA5990P

SIP For WLAN/BLUETOOTH/FM Radio Tuner

Rev.1.4–08.2012

1 General Description

RDA5990P integrates RDA5990,PowerAmplifier and antenna switch into one chip and is optimized for mobile applications. WLAN, Bluetooth and FM can work simultaneously and independently, with low power consumption levels target to battery powered devices. For the highest integration level, the required board space has been minimized and customer cost has been reduced. Manufacturers can easily and fast integrate RDA5990P on their product to enable a rapid time to market.

RDA5990P uses a compact 7*7mm 48-pin QFN package.

1.1 WLAN Features

- CMOS single-chip fully-integrated radio, PHY and MAC
- Single-band 2.4GHz IEEE 802.11b/g
- Support WEP, WPA/WPA2, WAPI
- WAPI hardware accelerated
- Industry Standard QoS schemes(802.11e,WMM) support
- Shared Bluetooth and WLAN receive signal path
- Shared Bluetooth and WLAN crystal
- Build-In IEEE 802.15.2 coexistence scheme
- Support host interfaces: SDIO v1.2, SPI
- Advance sleep and wakeup for power saving
- Smallest WLAN solution footprint
- No external EEPROM needed
- Support battery voltage range from 3v to 5v

1.2 Bluetooth Features

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth 2.1 + EDR specification
- Bluetooth Piconet and Scatternet support
- ARM7-based mcu with on-chip ROM and RAM
- Meet class 2 and class 3 transmitting power requirement, support class1 operation with external power amplifier
- Provides +10dbm transmitting power
- NZIF receiver with -90dBm sensitivity
- Battery power supply directly with internal LDO
- Support DCXO with internal oscillator circuit
- Up-to 4Mbps high speed UART HCI support
- Support AFH
- Build-In 3-wire WIFI Co-existence handshake signals
- Low power consumption
- Minimum external component
- Internal 32k LPO.

1.3 FM Features

- CMOS single-chip FM receiver/transmitter
- Low power consumption
  - Total current consumption lower than 20mA at 3.0V power supply
- Support worldwide frequency band
  - 50 -115 MHz
- Support flexible channel spacing mode
  - 100KHz, 200KHz, 50KHz and 25KHz
- Support RDS/RBDS
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC) Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control
- Line-level analog output voltage
- I2C control bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 1.8 to 5.5 V operation voltage

1.4 Applications

- Mobile handset
- MP3,MP4 and PMP
- PDA
- Cordless phone

2 Table of Contents

SIP For WLAN/BLUETOOTH/FM Radio Tuner **1**
- **1.1 WLAN Features** **1**
- **1.2 Bluetooth Features** **1**
- **1.3 FM Features** **1**
- **1.4 Applications** **1**

2 Table of Contents **2**
3 Block Description **3**
4 WLAN Section Electrical Characteristics **4**
6 WLAN Section Radio Characteristics **5**
7 Pins Description **7**
8 Application Circuit **10**
9 Package Physical Dimension **11**
10 PCB Land Patter **12**
11 Change List **14**
12 Contact Information **15**

3 Block Description

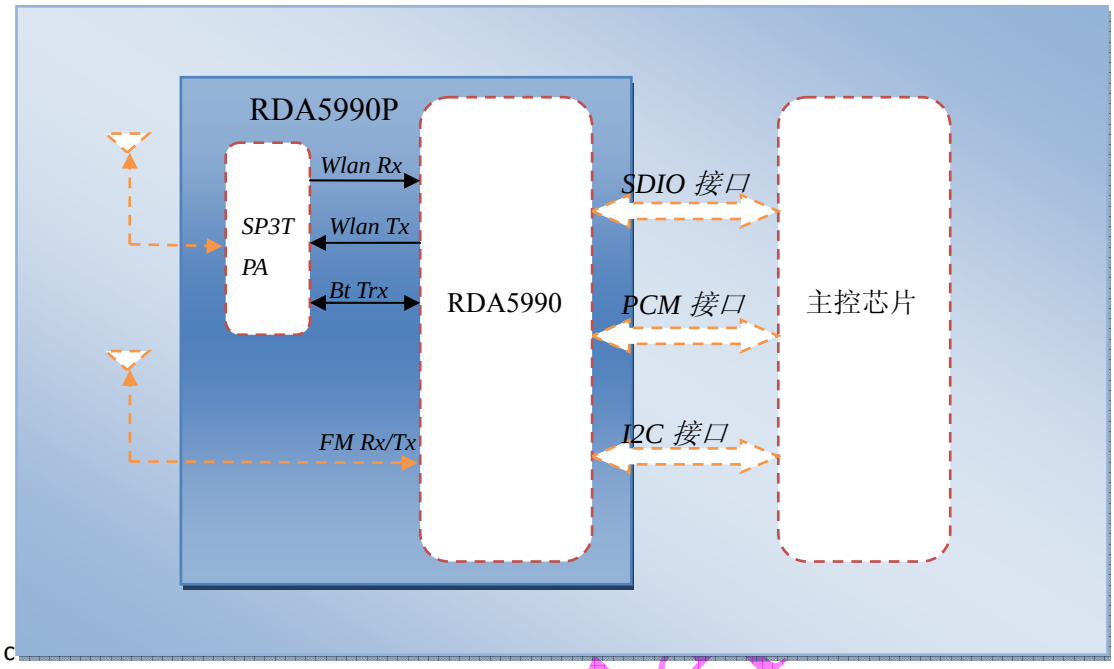


Figure3-1. RDA5990P Block Diagram

RDA5990P is a SIP chip, includes RDA5990, PowerAmplifier and antenna switch.

4 WLAN Section Electrical Characteristics

Table 5-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage from battery or LDO	3.3	4.0	4.2	V
T_{amb}	Ambient Temperature	-20	27	+50	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Notes:

1. VIO=1.8~3.3V

Table 5-2 WLAN Power Consumption(Ivbat+Ivio):

(VBAT = 3.6 V, VIO = 2.8V, T_A = +27℃, DCDC mode unless otherwise specified)

DESCRIPTION	MIN	TYP	MAX	UNIT
OFF(FM,BT,WIFI OFF)		7		uA
Deep Sleep		400		uA
Associated State		96		mA
Rx		127		mA
Tx		150		mA

Table 5-3 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-20		+80	°C
I_{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		VIO+0.3	V
V_{lna}	LNA Input Level			+10	dBm

6 WLAN Section Radio Characteristics

Table 6-1 WLAN 2.4 GHz Receiver Performance Specifications

(VBAT = 3.6 V, TA = 27°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Frequency range			Channel 1	-	Channel 14	
Rx Sensitivity (8%PER for 1024 octet PSDU) at WLAN RF port		1 Mbps DSSS	-90	-93	/	dBm
		2 Mbps DSSS		-91		dBm
		5.5 Mbps DSSS		-90		dBm
		11 Mbps DSSS		-89		dBm
Rx Sensitivity (10%PER for 1024 octet PSDU) at WLAN RF port		6 Mbps OFDM		-89		dBm
		9 Mbps OFDM		-87		dBm
		12 Mbps OFDM		-87		dBm
		18 Mbps OFDM		-85		dBm
		24 Mbps OFDM		-82		dBm
		36 Mbps OFDM		-79		dBm
		48 Mbps OFDM		-73		dBm
		54 Mbps OFDM		-73		dBm
Maximum Receive Level @2.4GHz		@1,2 Mbps(8% PER,1024octets)		10		dBm
		@5.5,11 Mbps(8% PER,1024octets)		5		dBm
		@6-54 Mbps(10% PER,1024octets)		2		dBm
Adjacent channel rejection DSS (Difference between interfering 1024 Octet PSDU with desired signal level As specified in Condition/Notes)		Desired and interfering signal 30 MHz apart				
		2 Mbps DSS	35	38		dB
		Desired and interfering signal 25 MHz apart				
Adjacent channel rejection DSS (Difference between interfering 1024 Octet		11Mbps DSS	35	36		dB
Adjacent channel rejection OFDM (Difference between interfering and desired signal (25MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in condition /Notes)		6 Mbps OFDM	16			dB
		9 Mbps OFDM	15			dB
		12 Mbps OFDM	13			dB
		18 Mbps OFDM	11			dB
		24 Mbps OFDM	8			dB
		36 Mbps OFDM	4			dB
		48 Mbps OFDM	0			dB
		54 Mbps OFDM	-1			dB
Maximum receiver gain				80		dB

Table 6-2 WLAN 2.4 GHz Transmitter Performance Specifications

(VBAT = 3.6 V, TA = 27°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
802.11b Transmitter						
Frequency range			Channel 1	-	Channel 14	MHz
Tx Power Level		Mask Compliant DSS/CCK output power ①		18		dBm
Frequency tolerance			-5	1	5	ppm
Spectrum Mask		11MHz to 22MHz			40	dBr
		22MHz to 50MHz			50	dBr
Modulation accuracy		All data rate		6	10	%
Time for power up				1.5		us
Time for power dowm				1.5		us
802.11g Transmitter						
Frequency range			Channel 1	-	Channel 14	MHz
Tx Power Level		EVM Compliant OFDM output power②		14		dBm
Frequency tolerance			-5	1	5	ppm
Modulation accuracy		All data rate		-30	-27	dB
Spectrum Mask		At 11 MHz offset				dBr
		At 20 MHz offset				dBr
		At 30 MHz offset				dBr

7 Pins Description

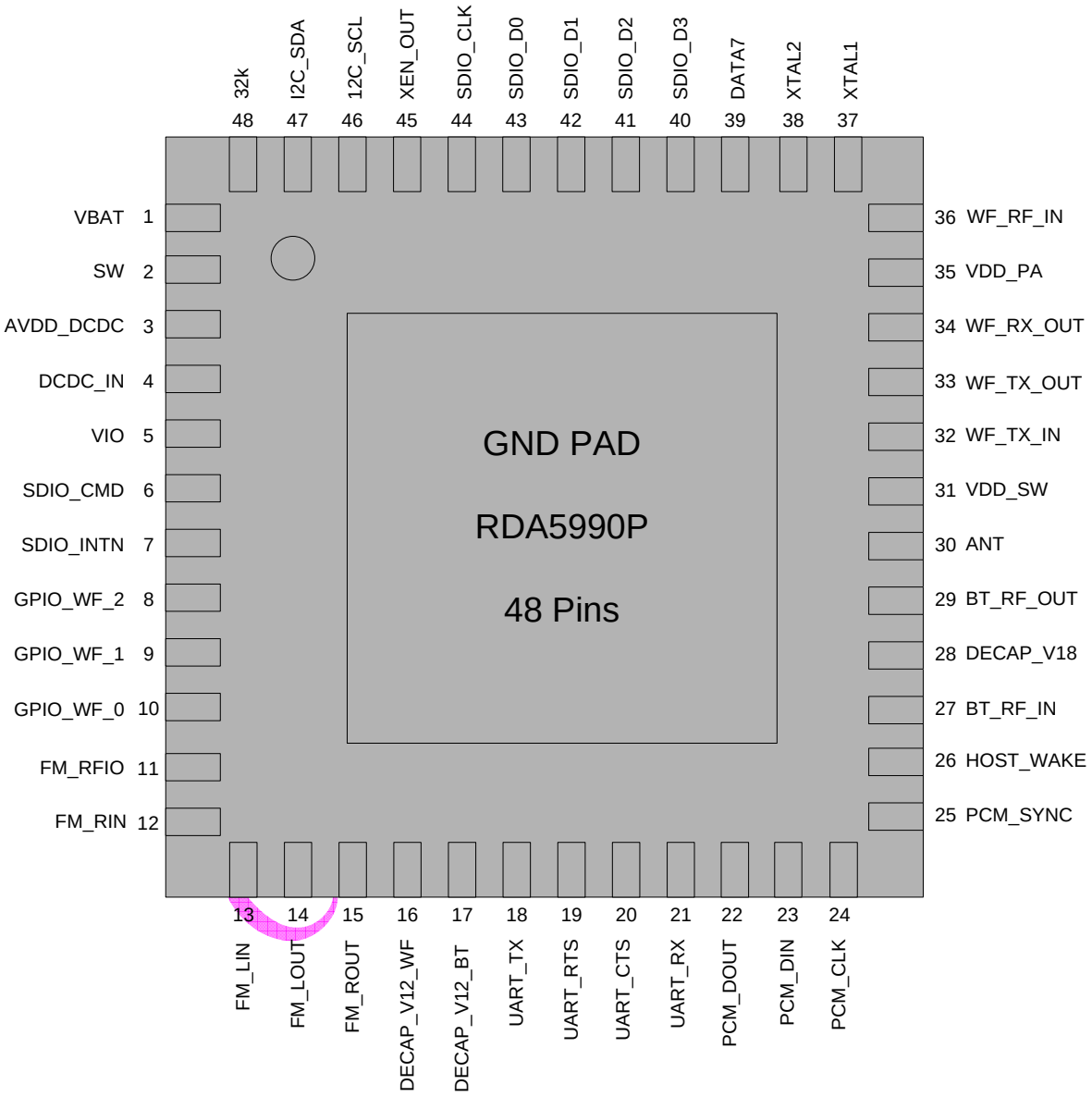


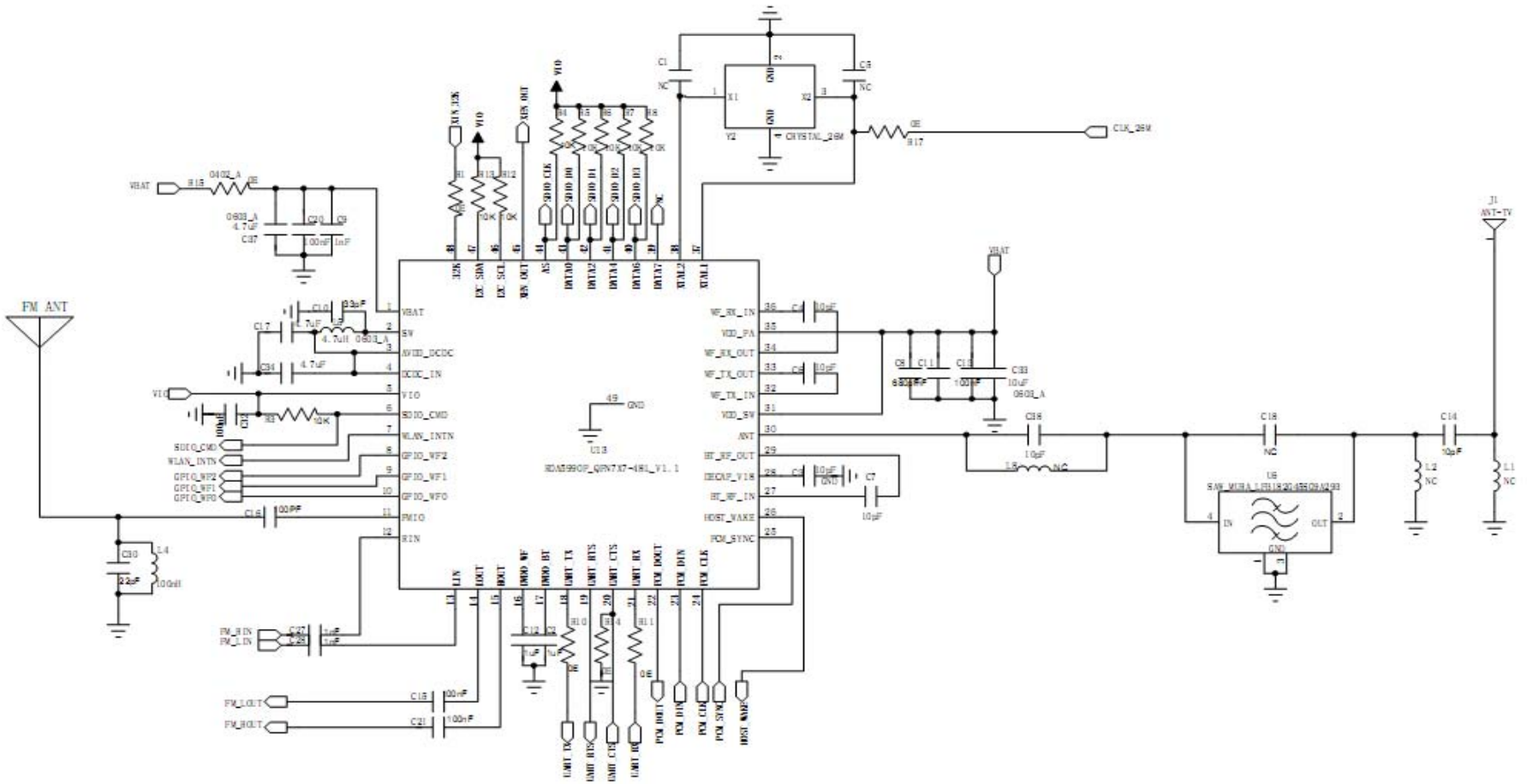
Table 7-1 RDA5990P Pins Description(7X7 48P)

PIN	NO.	DESCRIPTION
VBAT	1	Power supply
SW	2	Internal DC/DC switch voltage output
AVDD_DCDC	3	Analog voltage output, connected with decouple capacitor
DCDC_IN	4	DC/DC voltage output, connected with decouple capacitor
VIO	5	IO power supply
SDIO_CMD	6	SDIO Interface command
SDIO_INTN	7	WLAN int to host
GPIO_WF_2	8	Programmable I/O,NC Should be not connected
GPIO_WF_1	9	Programmable I/O,NC Should be not connected
XEN_IN	10	Clock request in, connected to bb xen_out for one of clock share modes; or tie gnd
FM_RFIO	11	FM radio signal,INOUT
FM_RIN	12	FM right audio input
FM_LIN	13	FM left audio input
FM_LOUT	14	FM left audio output
FM_ROUT	15	FM right audio output
DECAP_V12_WF	16	WIFI Digital voltage output, connected with decouple capacitor
DECAP_V12_BT	17	BT Digital voltage output, connected with decouple capacitor
UART_TX	18	UART data output
UART_RTS	19	UART ready to send
UART_CTS	20	UART clear to send
UART_RX	21	UART data input
PCM_DOUT	22	Synchronous data output
PCM_DIN	23	Synchronous data input
PCM_CLK	24	Synchronous data clock
PCM_SYNC	25	Synchronous data sync
HOST_WAKE	26	BT output to wakeup host
BT_RF_IN	27	
DECAP_V18	28	Analog voltage output, connected with decouple capacito
BT_RF_OUT	29	
ANT	30	ANT for WIFI,BT
VDD_SW	31	
WF_TX_IN	32	
WF_TX_OUT	33	
WF_RX_OUT	34	
VDD_PA	35	
WF_RX_IN	36	
XIN	37	For 26Mhz crystal input or external clock input
XTAL	38	For 26Mhz crystal input
NC	39	Should be connected GND
SDIO_D3	40	SDIO Interface data3
SDIO_D2	41	SDIO Interface data2
SDIO_D1	42	SDIO Interface data1
SDIO_D0	43	SDIO Interface data0
SDIO_CLK	44	SDIO Interface clk
XEN_OUT	45	Clock request output
I2C_SCL	46	I2C interface Clock signal
I2C_SDA	47	I2C interface Data signal
XIN_32K	48	32.768K clock input or external 32.768K crystal

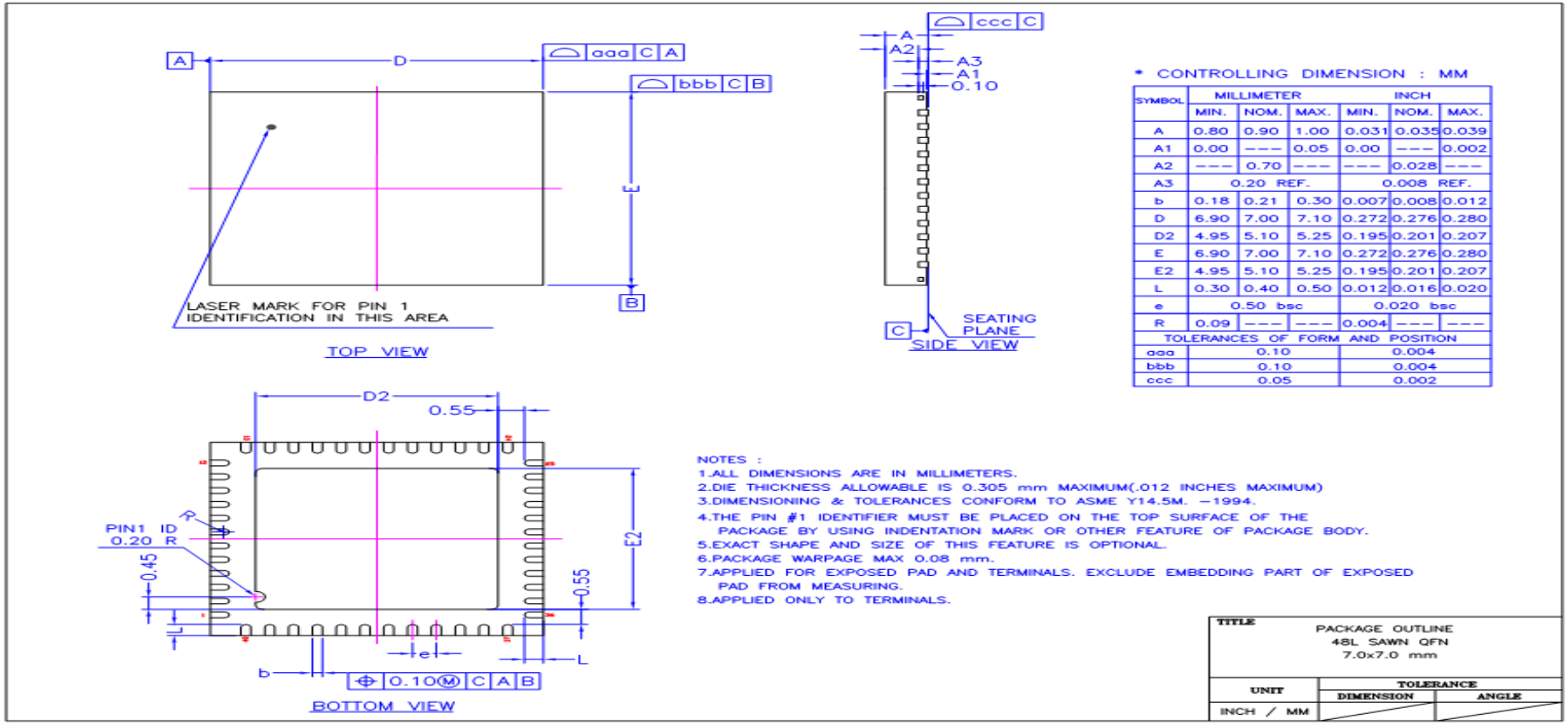
Table 7-2 RDA5990P IO power domain

PIN	NO.	POWER DOMAIN
SDIO_D3	40	DVDD_VIO
SDIO_D2	41	DVDD_VIO
SDIO_D1	42	DVDD_VIO
SDIO_D0	43	DVDD_VIO
SDIO_CLK	44	DVDD_VIO
SDIO_INTN	7	DVDD_VIO
GPIO_WF_2	8	DVDD_VIO
GPIO_WF_1	9	DVDD_VIO
UART_TX	18	DVDD_VIO
UART_RTS	19	DVDD_VIO
UART_CTS	20	DVDD_VIO
UART_RX	21	DVDD_VIO
PCM_DOUT	22	DVDD_VIO
PCM_DIN	23	DVDD_VIO
PCM_CLK	24	DVDD_VIO
PCM_SYNC	25	DVDD_VIO
HOST_WAKE	26	DVDD_VIO
XIN	37	300MV—2V
XTAL	38	
XIN_32K	48	300MV—2V
XEN_IN	10	DVDD_VIO
XEN_OUT	45	DVDD_VIO
I2C_SCL	46	DVDD_VIO
I2C_SDA	47	DVDD_VIO

8 Application Circuit



9 Package Physical Dimension



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.00	---	0.002
A2	---	0.70	---	---	0.028	---
A3	0.20 REF.			0.008 REF.		
b	0.18	0.21	0.30	0.007	0.008	0.012
D	6.90	7.00	7.10	0.272	0.276	0.280
D2	4.95	5.10	5.25	0.195	0.201	0.207
E	6.90	7.00	7.10	0.272	0.276	0.280
E2	4.95	5.10	5.25	0.195	0.201	0.207
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure9-1illustratesthepackage details for the RDA5990. The package is lead-free and RoHS-compliant.

10 PCB Land Patter

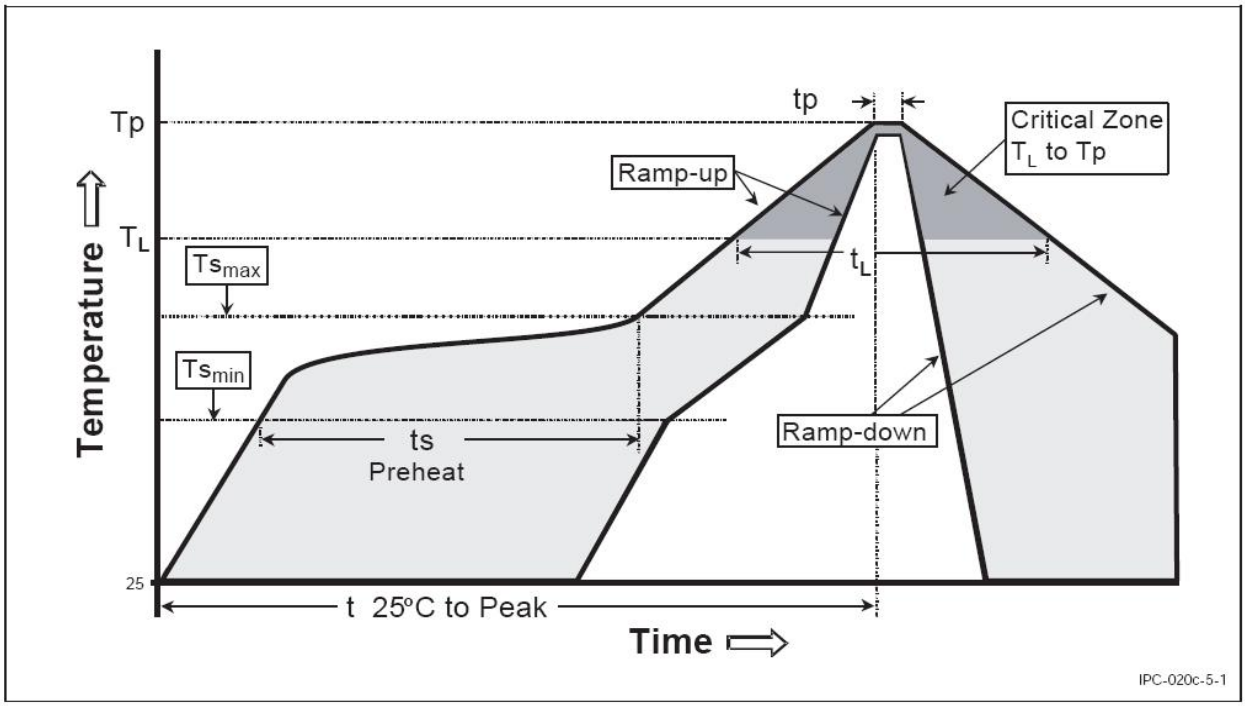


Figure17-1.Classification Reflow Profile

Table 17-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 9-2	See Table 9-3
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 17-2 Pb-free Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 17-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 17-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table17-1, 17-2, 17-3 whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated biphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

11 Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	02/28/2012	Juntao Miao	draft
V1.1	02/29/2012	Juntao Miao	Update Package Physical Dimension
V1.2	03/29/2012	Juntao Miao	Revise some text error
V1.3	04/21/2012	Juntao Miao	Add pin map and IO power domain
V1.4	08/12/2012	Juntao Miao	

12 Contact Information

RDA Microelectronics, Inc.

Suite 302 Building 2, 690 Bibo Road Pudong District, Shanghai
Tel: 86-21-50271108
Fax: 86-21-50271099
Postal Code: 201203

Suite 1108 Block A, e-Wing Center, 113 Zhichun Road Haidian District, Beijing
Tel: 86-10-62635360
Fax: 86-10-82612663
Postal Code: 100086

2501 Room, District A, XiNian Center, 6021 ShenNan Road, Nanshan District, Shenzhen.
Tel: 86-755- 86187018
Fax: 86-755- 33395366
Postal Code: 518057